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Flip Chip Bumping & Assembly

Hermann Oppermann
Fraunhofer IZM, Berlin
Gustav-Meyer-Allee 25
13355 Berlin
Tel.: +49 (0)30 46403-163
email: oppermann@izm.fhg.de
Flip Chip Bumping & Assembly

• Bumping: Wafer Level
• Bumping: Single Chip
• SMT compatible flip chip assembly
• SMT non-compatible flip chip assembly
• SMT like assembly for advanced products
Flip Chip Assembly

- face down assembly of bare dice
  - shortest interconnection, highest I/O counts
  - high electrical performance
  - smallest footprint
  - high reliability
Flip Chip Market by Technology

Total : 4,112 Wafers

2000

Total : 24,600 Wafers

2005

Source: Prismark
Bumping by Electroplating
### Flip Chip Bumping Technology - Overview # 1

<table>
<thead>
<tr>
<th>Bump</th>
<th>Wafer</th>
<th>Wafer Size</th>
<th>UBM</th>
<th>Bumping Technology</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Au</td>
<td>Si GaAs</td>
<td>4&quot; - 8&quot;</td>
<td>Ti:W / Au</td>
<td>Electroplating</td>
<td>TAB / TC, Opto, RF, Telecom.</td>
</tr>
<tr>
<td>AuSn</td>
<td>GaAs InP Si</td>
<td>3&quot; - 6&quot;</td>
<td>Ti:W / Au</td>
<td>Electroplating</td>
<td>FC, Opto, RF</td>
</tr>
<tr>
<td>PbSn 60</td>
<td>Si</td>
<td>4&quot; - 8&quot; (12&quot;)</td>
<td>Ti:W/Cu/ep-Cu Electroless Ni/Au Ni:V/Cu Cr/Cu Ti/Ni</td>
<td>Electroplating Printing Printing, ECD</td>
<td>FC, Memory, RF, Telecommunication</td>
</tr>
<tr>
<td>PbSn 5</td>
<td>Si</td>
<td>6&quot; - 8&quot;</td>
<td>Cr/Cu Ti:W/ CU</td>
<td>Evaporation ECD</td>
<td>FC, Automotive, Processor</td>
</tr>
<tr>
<td>AgSn</td>
<td>Si GaAs</td>
<td>4&quot; - 8&quot; 3&quot; - 6&quot;</td>
<td>Ti:W/Cu/ep-Cu NiV CrCu</td>
<td>Electroplating</td>
<td>FC, Memory, Telecommunication</td>
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<tr>
<td>CuSn</td>
<td>Si</td>
<td></td>
<td></td>
<td>in development</td>
<td></td>
</tr>
</tbody>
</table>
PbSn Solder Bump Structure

- wettable metallization (ep-Cu)
- plating base (Cu)
- adhesion layer & diffusion barrier (Ti/W)
- passivation (SiO2, Si3N4, SiON)
- VO-pad (Al)
- chip (Si)
Under Bump Metallization - UBM

**UBM**

**Adhesion-Layer & Diffusion Barrier**
- hermetic coverage of the chip pad
- good adhesion to Al chip pad
- minimum interdiffusion between bump metal and chip pad
- low degradation during temperature cycles imposed during reflow, bonding
- low internal stress
- low contact resistance

**Solder Base**
- sufficient wettability to the solder
- tolerable formation of intermetallics at the interface

**Solder** (e.g. PbSn63, PbSn5)
- mechanical contact to substrate
- stand-off chip-substrate
- good electrical contact
- high creep resistance to improve reliability under thermal loading
- high ductility to minimize mechanical stress due to different CTE of substrate and chip
Processflow - Gold Bumping

- **Sputtering**
- **Photo-lithography**
- **Electroplating**
- **Etching**

**Resist opening**
35 μm x 35 μm
thickness: 30 μm

**Gold bumps**
70 μm x 70 μm
space: 30 μm

Fraunhofer IZM
Institut Zuverlässigkeit und Mikrointegration

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Wafer-Bumping using Electroplating

Bumping-Service
Prototyping, Low-Volume Production, R&D
Engineering for Flip Chip, COB, TAB and COG Applications

Materials:
- Gold, Copper, Nickel
- Solder: Pb40Sn60, Pb95Sn5, AuSn, (AgSn)

Wafer Size: 4", 5", 6", 8"

Bump Size:

<table>
<thead>
<tr>
<th>Bump</th>
<th>footprint (µm)</th>
<th>pitch (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Au/AuSn</td>
<td>min. 15 x 15</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>typ. 80 x 80</td>
<td>150</td>
</tr>
<tr>
<td>PbSn</td>
<td>min. 20 x 20</td>
<td>30</td>
</tr>
<tr>
<td>(AgSn)</td>
<td>typ. 80 x 80</td>
<td>150</td>
</tr>
</tbody>
</table>

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
AuSn Bumping

Before and after reflow on InP-Laser

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages
phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Solder Bumping Pb40Sn60

PbSn60 Solder Bumps (diameter: 25 µm; pitch 50 µm)
UBM: Ti:W/Cu / ep.Cu (5µm)

after electroplating  

after Reflow
Production Equipment @ Fraunhofer IZM for Waferlevel Packaging up to 200 mm Wafer

RIE 1107
Matrix
Unaxis
Spin Coater ACS 200
Karl Süss

Mask Aligner MA 200
Karl Süss

Sputtertool LLS 802
Unaxis

Equinox Plater
Semitool
Copper/Solder-Plating Tool - Equinox
Bumping by
UBM deposition and
solder paste printing
Electroless Bumping - Advantages

- no masks required
- no sputtering
- high throughput
- suitable for soldering and adhesives
- low investment required
- extendable to 300 mm wafers
Electroless Bumping - Process Flow

- Backside Coating
- Passivation Cleaning
- Aluminum Cleaning
- Zincating
- Electroless Nickel
- Immersion Gold
- Coating Removal

Electroless Ni/Au UBM

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages
phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Electroless Ni UBM

- 50 µm pitch full array
- 5 µm height
- x-ray pixel detector
Sputter UBM for solder paste printing

Sputter metals: Ni:V/Cu/Au
               Cr/Cu/Au
               Ti/Ni/Au

Patterning: Lift-off or etching

Equipment: Sputter tool
           spin coater
           mask aligner
Solder Bumping by Stencil Printing - Process Flow

solder bumps
- solder: PbSn63
- UBM: 5 µm Ni
- height: 95 µm
- pad: 100x100 µm²
Principle of Solder Paste Stencil Printing on Wafer Level

- Squeegee
- Solder Paste
- Stencil Aperture
- IC Metallization
- Wafer
Flip Chip Solder Joints On FR - 4 Boards

Stencil Printing of Solder Paste on Wafers (4“) with Electroless Nickel/Gold Metallization

Increasing melting point

Sn/Pb - 63/37
Sn/Bi/Cu - 90/9.5/0.5
Sn/Ag - 96.5/3
Sn/Cu - 97/3

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Immersion Soldering for Ultra Fine Pitch Bumping

- Wafer with Ni bumps
- Wafer with solder caps on Ni bumps
- Equipment for wafer handling
- Basin
- Solder reservoir
- Organic liquid

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages
phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
AuSn Bumping

solder paste printing & reflow

immersion soldering
Single Chip Bumping
Stud Bumping

Advantages:

- maskless process
- wire bonder
- very flexible
- suitable for single chip and substrates

Bumping procedure:
Cl: wire-clamp,
C: capillary

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Stud Bumping of Au

Other metal studs: Ag, Pd, Pt, Cu

75µm Diameter

Stacked Ball Bumps

Hardness of Ballbumps

20-50 HV
50-70 HV
70-80 HV
World Record in Au Stud Bumping?
World Record in Thermocompression Bonding?

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Assembly compatible to SMT
Flip Chip and SMD Assembly

- solder bumps PbSn63, 100 µm
- FR4 boards with solder mask and Ni/Au finish
- fluxing of flip chip sites
- reflow under nitrogen
- underfill dispense and cure

compatible to SMD assembly
Schematics of Flip Chip Underfill

Underfill application at die edge, different dispense patterns

SEM-Image of a cross section of an underfilled Flip Chip
Flip Chip Assembly Line

FC / SMD Assembly Line
- Stencil printer
- SMD & Flip Chip placer
- Reflow oven
- Dispenser

flip chip and SMD assembly line
No-Flow Underfill

- Underfill Dispensing
- Flip Chip Placement
- Reflow Cure
SMT compatible Flip Chip Technology: Consumer Product

Electronic Toothbrush

board with 63 substrates

single substrate with SMD´s and flip chip

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
SMT compatible Medical Product

New Product: Pacemaker (Biotronik) - WL-CSP on Dycostrate™

Old Version
Multilayer Ceramic SMD, Laserweld & Wirebonding

New Version
WL-CSP on Rigid-Flex Dycostrate™ Board & Solder Ball
New Product: Pacemaker (Biotronik) - WL- CSP on Dycostrate™

MCM - CSP’s for Pace Makers: Specifications

<table>
<thead>
<tr>
<th>IC number &amp; type</th>
<th>Hood</th>
<th>Ira</th>
<th>Tria</th>
<th>Virgin</th>
</tr>
</thead>
<tbody>
<tr>
<td>chip size (mm²)</td>
<td>2x2</td>
<td>3x4</td>
<td>5x7</td>
<td>9x9</td>
</tr>
<tr>
<td>pitch (original) (µm)</td>
<td>140</td>
<td>180</td>
<td>180</td>
<td>200</td>
</tr>
<tr>
<td>pitch after redistribution (µm)</td>
<td>800</td>
<td>1000</td>
<td>800</td>
<td>800</td>
</tr>
<tr>
<td>No. of Balls</td>
<td>9</td>
<td>30</td>
<td>35</td>
<td>108</td>
</tr>
</tbody>
</table>

Chip - Set for Pacemakers

- Redistribution using Photo-BCB/Cu
- Bumping by Stencil Printing

SMT compatible Medical Product

New Product: Pacemaker (Biotronik) - WL- CSP on Dycostrate™

Chip Interconnection Technologies and Advanced Packages

Dr. Hermann Oppermann

Fraunhofer Institute for Reliability and Microintegration

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Wafer Level Redistribution

Reduce substrate and assembly cost

Electroless Cu Lines

- electroless Cu lines
- 6 µm thickness, 40 µm width
- specific resistance 2.7 ± 0.1 µΩ cm
- equivalent to 4.5 mΩ/□
SMT compatible Medical Product, non-implantible
Assembly barely compatible to SMT
Flip Chip Using Adhesives: Methods

**Isotropic Conductive**

1. IC
2. Syringe

ICA
Bondpad
Substrate
Underfiller
Temperature

**Anisotropic Conductive**

IC
Gold Bump
ACA
Substrate
Bondpad
Load + Temperature

**Non-Conductive**

IC
Mech. Gold Bump
NCA
Substrate
Bondpad
Load + Temperature

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Thermode Bonding

- Heating rate: 100 K/s
- Bond force: < 40g
- Flexible substrate

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Flip Chip for RF Module (Decorrelator at 26 GHz)

Substrate bumping:
bump diameter: 100 µm
bump height: 60 µm

organic substrate with PTFE layer

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Flip Chip for High Frequency Applications: Chip on Chip

TC bonding of InGaAsP Photodiode array on GaAs Preamplifier using Au stud bumps
Thermal and Electrical Bumps

thermocompression bonding of electroplated Au bumps on top of a dielectric bridge filled with BCB
• Optical beam level and mirror designed into silicon bench
• electrical signal lines defined on silicon
• less components (no posts, no additional bench for fiber)
• only one solder type (AuSn)
• solder deposited on silicon bench or on components
• Precise mounting of monitor diode to the etched mirror (10 µm)
• Precise mounting of laser diode to the V-grooves (1 µm)
• laser p-side down preferred
• active or passive fiber alignment
Cross-section:

View into the V-groove to the mirror

PIN diode soldered with AuSn layers of 3.5 µm thickness

Pin diode in flip chip technology
Thermode Bonding

Karl Suss FC150

GaAlAs-Chip  silicon-substrate  arm-tool  chuck-tool

alignment  force

GaAlAs-Chip  silicon-substrate  chuck-tool

heat  arm-tool

heat
Flip Chip Bonder

Feeder Module:
- transfer robot with loading and flipping carrousel
- waffle pack support
- wafer frame support (t.b.d)
- tape-on-reel support (t.b.d)

Process Module:
- up to 350 parts per hour
- resolution 1µm
- automatic alignment
- alignment accuracy 2µm
- universal bonding arm (0.1 to 50 kg)
- IR heating system (15 °C / sec)
- fast pulse heating system (t.b.d.)
... but assembly processes similar to SMT
Rx and Tx Modules

Flip Chip Self-Alignment

InP laser diode  Flip chip PIN diode  Low cost flip chip:

- Au+Sn wafer bumping
- solder reflow on wafer
- singulation
- tolerant pick & place
- fluxless „SMT“ reflow
- self-alignment

Christine Kallmayer

Fraunhofer Institute for Reliability and Microintegration

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163, FAX +49 30 46403-161, email: oppermn@izm.fhg.de
100 Gb/s Receiver Module

**RF compatible approach**

- **Ultra-fast receiver diode** (HHI)
- **Wafer Bumping Au, AuSn fluxless assembly** (IZM)
- **Thinfilm substrate** Si/Cu/BCB/Au/BCB with shielded co-planar WG (IZM)
- **Fiber coupling and module housing** (HHI)

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Dr. Hermann Oppermann
Chip Interconnection Technologies
phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de

Fraunhofer
Institut
Zuverlässigkeit und Mikrointegration

Fraunhofer
Institut
Nachrichtentechnik Heinrich-Hertz-Institut
76 GHz Radar Frontend Sensors  Flip Chip Self-Alignment

Electroplated Au-Sn bumps

Au-Sn bumps after reflow

X-ray image of assembly

Christine Kallmayer / Matthias Hutter

Fraunhofer
Institut
Zuverlässigkeit und Mikrointegration

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Pump combiner module

4 integrated laser chips with pump combiner on a planar lightguide circuit (PLC)

Metal pad on PLC and power line

Bond wire

2mm pitch

Laser chip in cavity

2.4mm

Self-alignment
Pump combiner module

- Waveguide with FBG
- etched stopper
- Flip chip mounted laser in self-aligned position contacting etched stoppers
- Metall Pad
- (530±0,25)µm
- Cavity in PLC

Self-alignment

- Laser chip (Cross View)
  - 500µm
- Laser Near Field
- Laser chip (Top View)
- Alignment marks
- Metall Pad
- 550µm

Fraunhofer Institut Zuverlässigkeit und Mikrointegration

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Self-Alignment in XZ direction

Placement laser on PLC

Laser chip

Step height 5µm

Silica Upper Cladding 15µm

Silica WG Layer

6µm

Silica Lower Cladding 20µm

Silicon base of PLC

Laser Near Field

laser pad

solder

solder

stopper on laser chip

stopper on silicon bench

Dr. Hermann Oppermann

Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
Silicon base of PLC

Silica Lower Cladding 20µm

Silica Upper Cladding 15µm

Silica WG Layer 6µm

Silica Lower Cladding 20µm

Pump combiner module
Self-Alignment in XZ direction

Alignment force

Laser chip

Laser Near Field

Step height 5µm
Highspeed Optical Switches: 64x64

- SM output
- Focus adjusted for 1550nm
Highspeed Optical Switches: 64x64

- 64x64 strictly non-blocking switch
- Optical Phase Array Technology
- Net switch-over time < 20nsec
- Fully integrated in IP router
- Over a year in production
- Telecordia compliance

presented by CHIARO at OFC March 2002
and by CHIARO and AT&T at LEOS 2002
Highspeed Optical Switches: 64x64

Assembly Process:
• Pick & Place
• Soldering in oven

GaAs chip with 2048 integrated waveguides

Optical fiber array and microlenses
Highspeed Optical Switches: 64x64

GaAs chip, dimension 31x12 mm² with 2048 integrated waveguides and more than 2500 AuSn bumps

Single deflector 128 waveguides

18 deflectors
Flip chip reflow soldering with electroplated AuSn solder bumps using self-alignment on 25-layer ceramic (Kyocera)

- Waveguides
- Dielectric layer
- Waveguide contact via
- Substrate contact

Large bumps used to compensate shrinkage and flatness of ceramic
High Brightness Flip Chip LED

**Advantages:**
- no wire bond
  - high reliability
  - easier, insensible handling
  - dens packaging
  - good optical properties
- good heat transfer
- high brightness
  - 60 mW optical
  - 540 mW heat
  - active area: 250 x 250 µm

**Goal:** surface mount device
High Brightness Flip Chip LED

Assembly

- chip gold metallization
- substrate tin metallization
- chip placed on substrate
- reflow

BSE image of a cross section of a LED assembly after reflow (C, 290°C)
High Brightness Flip Chip LED

Metallization

type

chip pad

A

6 μm Au

B

10 μm Au

C

10 μm Au

D

7 μm Au

5 μm Sn

substrate

10-16 μm Sn

4 μm Sn

Sn

Au

Au

3-5 μm Au

tin on substrate

tin on LED

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
High Brightness Flip Chip LED Metallization

- type A/B
- C
- D

Dr. Hermann Oppermann
Chip Interconnection Technologies and Advanced Packages

phone +49 30 46403-163,
FAX +49 30 46403-161,
email: oppermn@izm.fhg.de
High Brightness Flip Chip LED Assembly

SMT type pick & place and reflow at 320°C
High Brightness Flip Chip LED  Wafer Level Assembly

576 dice assembled on 4" Si wafer